CLAIMS:

1. An integrated display unit with:

- a display with a plurality of display elements (Dx) which are combined into a plurality of groups,

- a circuit arrangement for controlling the display with a plurality of switches (Sw1, Sw2, ...) which can be closed with a first clock signal and opened with a second clock signal, and with a plurality of inverters (In1, In2, ...), wherein the switches and inverters are connected in series in mutual alternation, such that

- each group of display elements (Dx) is connected to an output of an inverter (In1, In2, ...) each, and with

- at least one clock bus line (Φ1, Φ2) via which the first and the second clock signal are supplied in alternation to the first, third, fifth, etc. switch (Sw1, Sw3, Sw5, ...) of the series arrangement, and the second and the first clock signal are supplied in alternation to the second, fourth, sixth, etc. switch (Sw2, Sw4, Sw6, ...), so that after the application of a third clock signal to the input of the series arrangement, consecutively at a time at least one group of display elements (Dx) is activated.

2. An integrated display unit as claimed in claim 1, with a carrier on which the display elements (Dx) are arranged in the form of a display field, wherein the at least one clock bus line (Φ1, Φ2) extends along the edge of the display field.

3. An integrated display unit as claimed in claim 1, wherein the groups of display elements (Dx) are each formed by a row or a column of a matrix display.

4. An integrated display unit as claimed in claim 1, wherein the switches (Sw1, Sw2, ...) are each formed by an n-transistor, and the inverters (In1, In2, ...) are each formed by a parallel arrangement of a p-transistor and an n-transistor.

5. An integrated display unit as claimed in claim 1, wherein the groups of display elements (Dx) in the non-interlaced control of said groups are connected to respective outputs of the second, fourth, sixth, etc. inverter (In2, In4, In6, ...) of the series arrangement.

6. An integrated display unit as claimed in claim 5, wherein the groups of display elements (Dx) are the sampled rows or sampled columns of a matrix display.

7. An integrated display unit as claimed in claim 1, wherein the groups of display elements (Dx) for the interlaced control of said groups can each be connected via a converter (Um1, Um2, ...) to a fifth or sixth clock bus line (B1, A2) for the half-image switch-over, and the converters (Um1, Um2, ...) can each be switched over by means of a signal applied to the input and/or the output of the associated inverter (In1, In2, ...).

8. An integrated display unit as claimed in claim 7, wherein the converters (Um1, Um2, ...) are formed by two on/off switches each comprising a p- and an n-transistor.

9. An integrated display unit as claimed in claim 7, wherein the groups of display elements (Dx) are the sampled rows and/or the sampled scanning columns and/or the data rows and/or the data columns of a matrix display.